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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,050	11/29/2001	Andre Weimerskirch	US010422	5481
24737	7590	04/06/2005	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			DO, CHAT C	
			ART UNIT	PAPER NUMBER
			2193	
DATE MAILED: 04/06/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/998,050

Applicant(s)

WEIMERSKIRCH, ANDRE

Examiner

Chat C. Do

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-21 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/04/2005.
2. Claims 1-21 are pending in this application. Claims 1, 10, and 18 are independent claims. In Amendment, claims 1, 10, and 18 are amended. This Office action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8 and 10-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Epstein (U.S. 6,631,390).

Re claim 1, Epstein discloses in Figures 2A-2C as a first embodiment a method for generating a random number (abstract), comprising the steps operating a plurality of flip-flops a meta-stable state (e.g. primarily flip-flop 210 and then 240-242, col. 4 lines 8-16 and lines 48-55), each of the plurality of flip-flops connected to delay circuitry operable to violate set-up and/or hold times of the flip-flop so as to put the flip-flop in a meta-stable state (e.g. column 2 lines 54-61); generating a random bit if one of flip-flops enter meta-stable state (col. 3 lines 1-5); and preventing the generation of a random more than of plurality of flip-flops enter meta-stable state within a predefined time interval

(col. 4 lines 32-37 wherein if flip-flop 210 is not in meta-stage, than no mistake is generated and no random number is generated from circuit 260).

Re claim 2, Epstein further discloses in Figures 2A-2C as a first embodiment the flip-flops are driven in parallel (Figures 2B 240-242).

Re claim 3, Epstein further discloses in Figures 2A-2C as a first embodiment at least one of flip-flop is connected to least one other of flip-flops (Figure 2B wherein 210 is connected to 240-242).

Re claim 4, Epstein further discloses in Figures 2A-2C as a first embodiment the preventing step is performed by one or more exclusive or (XOR) circuits (250).

Re claim 5, Epstein further discloses in Figures 2A-2C as a first embodiment the generating step further comprises the step of choosing a random bit an output of one of flip-flops does not match an applied input (output of 250 as mistake signal).

Re claim 6, Epstein further discloses in Figures 2A-2C as a first embodiment the step of synchronizing an output of each of flip-flops (all flip-flop is driven with 230) with local clock source (230).

Re claim 7, Epstein further discloses in Figures 2A-2C as a first embodiment a synchronizing circuit that performs synchronizing step is less susceptible becoming meta-stable than flip-flops (col. 4 lines 50-60).

Re claim 8, Epstein further discloses in Figures 2A-2C as a first embodiment the step of a plurality of random bits to produce a random collecting number (260).

Re claim 10, it is a means claim of claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it is a means claim of claim 2. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, it is a means claim of claim 3. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 13, it is a means claim of claim 4. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 14, it is a means claim of claim 5. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 15, it is a means claim of claim 6. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 16, it is a means claim of claim 7. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 17, it is a means claim of claim 8. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 18, Epstein discloses in Figures 2A-2C as a first embodiment a method for generating a random number (abstract), comprising the steps operating a first flip-flop in a meta-stable state (210); and generating a random bit from an output of a second flip flop when first flip-flop is meta-stable state (242).

Re claim 19, it is has limitations cited in claim 4. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 20, it is has limitations cited in claim 6. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 21, it is has limitations cited in claim 8. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Allowable Subject Matter

5. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 01/04/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 9 for claims 1, 10, and 18 that the cited reference by Epstein discloses circuits containing one flip-flop intended to be driven into a meta-stable state along with a series of flip-flops intended to avoid entering the meta-stable state which operate to synchronize the output of the meta-stable flip- flop with another signal wherein the flip-flops of present invention are intended to enter into meta-stable states.

The examiner respectfully submits that the cited reference by Epstein clearly discloses, teaches, or suggests the flip-flops of present invention are intended to enter into meta-stable states in Figures and in column 2 lines 54-61.

7. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., multiple

instantiations of such circuitry or the ancillary circuits coupled to these multiple instantiations, that are used to detect the influence externally applied noise in page 9 third paragraph) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 1, 2005


KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100